

GaAs FET's Gate Current Behavior and its Effects on RF Performance and Reliability in SSPA's

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This paper presents a detailed experimental investigation of gate current limitation effects on power GaAs FET's rf performances. This limitation is accomplished entirely by dynamic compensation of the gate bias voltage. Effects of this current limitation on power added efficiency and output power performances have been examined through an extensive experimental investigation using active second-harmonic loading over the entire Smith chart. Comprehensive results are given and enable the determination of the optimal gate resistor value needed in the dc path for gate current limitation. Thermal runaway problem is also considered when selecting the gate resistor. The current limitation mechanism is analyzed in the case where the gate voltage is controlled in a feedback loop for linearization purposes. Measurements performed on a feedback linearized amplifier are presented and show the behavior of the gate current and its effects on intermodulation product levels.

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